

**RESPONSE UNDER 37 CFR 1.116  
EXPEDITED PROCEDURE  
EXAMINING GROUP 2817**

**PATENT**  
Attorney Docket No. 401251/TAKADA

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

ISHIDA et al.

Art Unit: 2817

Application No. 09/877,037

Examiner: S. Jones

Filed: June 11, 2001

For: **MATCHING CIRCUIT AND  
SEMICONDUCTOR DEVICE**

**PENDING CLAIMS**

13. A monolithic microwave integrated circuit (MMIC) comprising:  
a transistor having an input terminal and an insulating film around the transistor,  
affecting input capacitance of the transistor, the input capacitance changing directly with  
thickness of the insulating film; and  
a metal-insulator-metal (MIM) capacitor including two metal electrodes separated by  
part of the insulating film, one of the metal electrodes being connected to the input terminal of  
the transistor, capacitance of the MIM capacitor changing inversely with the thickness of the  
insulating film, whereby variations in the input capacitance of the transistor and the capacitance  
of the MIM capacitor due to variations in the thickness of the insulating film are compensated.

14. The MMIC according to claim 13 including a bias circuit connected in parallel with  
the MIM capacitor.

15. A monolithic microwave integrated circuit (MMIC) comprising:  
a transistor having an output terminal and an insulating film around the transistor,  
affecting output capacitance of the transistor, the output capacitance changing directly with  
thickness of the insulating film; and  
a metal-insulator-metal (MIM) capacitor including two metal electrodes separated by  
part of the insulating film, one of the metal electrodes being connected to the output terminal of  
the transistor, capacitance of the MIM capacitor changing inversely with the thickness of the

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insulating film, whereby variations in the output capacitance of the transistor and the capacitance of the MIM capacitor due to variations in the thickness of the insulating film are compensated.

16. The MMIC according to claim 14 including a bias circuit connected in parallel with the MIM capacitor.